IN THE CLAIMS

Please reinstate originally filed claims 1-3, 7 and 17 as added claims 21-25, respectively.

Please amend claim 4 as indicated below.

This listing of claims will replace all prior versions, and listings, of the claims in the Application.

Listing of Claims:

Claims 1-3 (cancelled)

Claim 4 (currently amended) The register file as recited in claim 21, ~~A register file comprising:~~

~~a plurality of register file cells coupled to a bit line;~~

~~a latch coupled to the bit line; and~~

~~an inverter coupled between an output of the latch and the bit line;~~

wherein the inverter is a tri-state inverter receiving a hold select signal to control operation of the inverter.

Claim 5 (original) The register file as recited in claim 4, wherein an output of the inverter is coupled to the bit line and wherein an input of the inverter is coupled to the output of the latch.

Claim 6 (original) The register file as recited in claim 5, wherein data is read out of the register array to be input into the latch.

Claim 7 (cancelled)

Claim 8 (original) A register file comprising:

a first plurality of cells coupled to a first local bit line;

a global bit line;

a first tri-state inverter coupled between the first local bit line and the global bit line, the first tri-state inverter controlled by a first local select signal;

a second plurality of cells coupled to a second local bit line;

a second tri-state inverter coupled between the second local bit line and the global bit line, the second tri-state inverter controlled by a second local select signal;

a latch with its input coupled to the global bit line; and

a third tri-state inverter coupled between an output of the latch and the global bit line, the third tri-state inverter controlled by a hold signal.

Claim 9 (original) The register file as recited in claim 8, further comprising:

an inverter coupled between the global bit line and the input of the latch.

Claim 10 (original) The register file as recited in claim 8, wherein when the third tri-state inverter is activated, the first and second local select signals are deactivated.

Claim 11 (original) A register file comprising:

a plurality of register file cells coupled to a bit line;

a latch coupled to the bit line; and

a transmission gate circuit coupled between an output of the latch and the bit line.

Claim 12 (original) The register file as recited in claim 11, further comprising:

an inverter coupled between the bit line and an input of the latch.

Claim 13 (original) The register file as recited in claim 11, wherein the output of the latch is an output of the register file.

Claim 14 (original) The register file as recited in claim 11, wherein the transmission gate circuit receives a hold select signal.

Claim 15 (original) The register file as recited in claim 14, wherein an output of the transmission gate circuit is coupled to the bit line and wherein an input of the transmission gate circuit is coupled to the output of the latch.

Claim 16 (original) The register file as recited in claim 15, wherein data is read out of the register array to be input into the latch.

Claim 17 (cancelled)

Claim 18 (original) A register file comprising:

a first plurality of cells coupled to a first local bit line;

a global bit line;

a first transmission gate coupled between the first local bit line and the global bit line, the first transmission gate controlled by a first local select signal;

a second plurality of cells coupled to a second local bit line;

a second transmission gate coupled between the second local bit line and the global bit line, the second transmission gate controlled by a second local select signal;

a latch with its input coupled to the global bit line; and

a third transmission gate coupled between an output of the latch and the global bit line, the third transmission gate controlled by a hold signal.

Claim 19 (original) The register file as recited in claim 8, further comprising:

an inverter coupled between the global bit line and the input of the latch.

Claim 20 (original) The register file as recited in claim 8, wherein when the third transmission gate is activated, the first and second local select signals are deactivated.

Claim 21 (new) A register file comprising:

a plurality of register file cells coupled to a bit line;

a latch coupled to the bit line; and

an inverter coupled between an output of the latch and the bit line.

Claim 22 (new) The register file as recited in claim 21, further comprising:

another inverter coupled between the bit line and an input of the latch.

Claim 23 (new) The register file as recited in claim 21, wherein the output of the latch is an output of the register file.

Claim 24 (new) The register file as recited in claim 21, wherein a multiplexor is not coupled between the bit line and the latch.

Claim 25 (new) The register file as recited in claim 11, wherein a multiplexor is not coupled between the bit line and the latch.